

TITLE 100G QSFP28 10km LR4 C-temp Transceivers	DOC No.	DTRX-220007
	REVISION : 01	AUTHORIZED BY : Mike Sun
	DATE : 2022.08.09	CLASSIFICATION : CONFIDENTIAL

1. SCOPE

QSFP28 transceiver modules are designed for use in 100 Gigabit Ethernet links over single mode fiber.

They are compliant with SFF-8665, INF-8438i and IEEE 802.3ba 100GBASE-LR4. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP28 MSA.

2. PRODUCT FEATURES

- Up to 10km reach for G.652 SMF
- Cooled 4x25Gb/s LAN WDM DML TOSA with optical MUX
- 4x25G Electrical Interface
- Single +3.3V power supply
- DDM function implemented
- 2 Wire Serial Interface for module management
- Maximum power dissipation < 4.5W
- Operating temperature range: 0°C ~ 70°C
- Compliant with RoHS6

3. PRODUCT DESCRIPTION

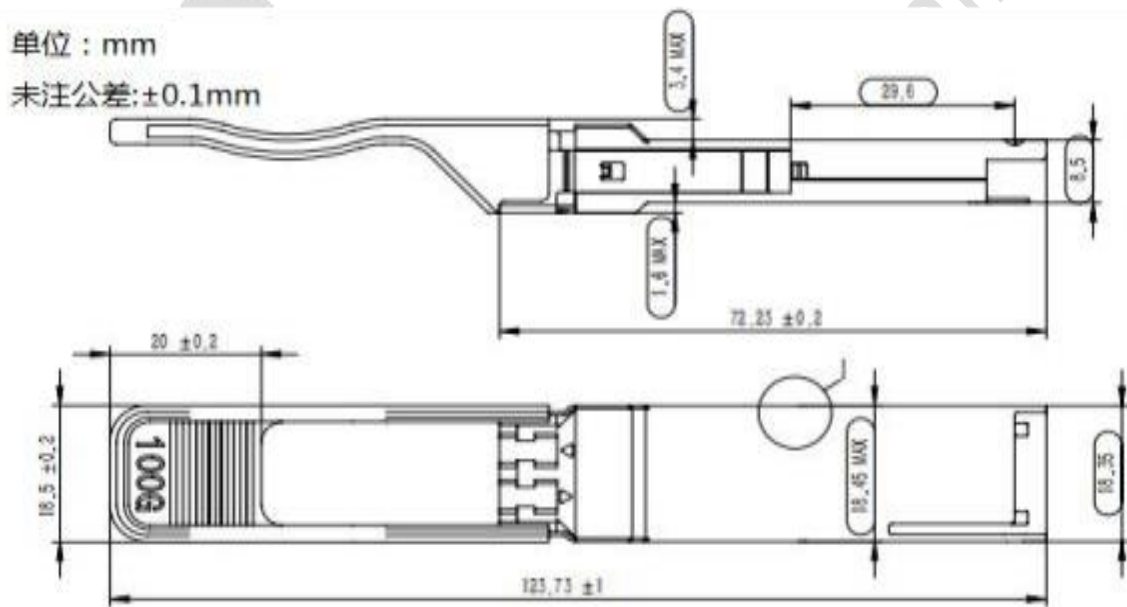
3.1 PRODUCT NAME AND SERIES NUMBER(S)

100G QSFP28 LR4 Transceiver

Part Number	Data Rate	Wavelength (nm)	Distance	Media	Power (dBm)	Sen. (dBm)	Connector	Tem.
P5800AEGCU10-1	100G	LAN WDM DFB 4	10km	SMF	-4.3 ~ 4.5	-8.6	LC	C

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3.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



Unit is millimeter. All dimensions are ± 0.1 mm unless otherwise specified.

4. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- Compliant with QSFP28 MSA (SFF-8665 V1.9)
- Compliant with IEEE 802.3ba
- 100GBASE-LR4 Ethernet

5. SUPPORT PROTOCOL

- IEEE 802.3ba
- QSFP MSA
- SFF-8636
- SFF-8661

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6. Absolute Maximum Ratings & Recommended Operating Conditions

Absolute Maximum Ratings				
Parameter	Symbol	Min.	Max.	Unit
Storage Temperature Range	Ts	oC	-40	85
Relative Humidity	RH	%	0	95
Maximum Supply Voltage	Vcc3	V	-0.5	4.0

Recommended Operating Conditions				
Parameter	Symbol	Min.	Max.	Unit
Operating Case Temperature Range	Tc	0	70	°C
Power Supply Voltage	Vcc	3.14	3.46	V
Bit Rate	BR		103.1	Gb/s
Bit Error Ratio	BER		10 ⁻¹²	
Max Supported Link Length	L		10	Km

Transmitter Optical Specification					
Parameter	Symbol	Min.	Typical	Max.	Unit
Signal Rate (Each Lane)	-	25.78125±100ppm			Gbps
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm
	L1	1299.02	1300.05	1301.09	nm
	L2	1303.54	1304.58	1305.63	nm
	L3	1308.09	1309.14	1310.19	nm
Total Average Launch Power	Pout			10.5	dBm
Transmit OMA per Lane	TxOMA	-5		5	dBm
Average Launch Power per Lane	TXPx	-4.3		4.5	dBm

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Optical Extinction Ratio	ER	3.5			dB
Side-Mode Suppression Ratio (SMSR)	SMSR	30			dB
Average launch power of OFF transmitter, per lane				-30	dBm
Relative Intensity Noise	RIN			-128	dB/Hz
Optical Return Loss Tolerance				20	dB
Transmitter Reflectance				-12	dB
Transmitter Eye Mask Definition {X1,X2,X3,Y1,Y2,Y3}				{0.25,0.4,0.45,0.25,0.28,0.4}	

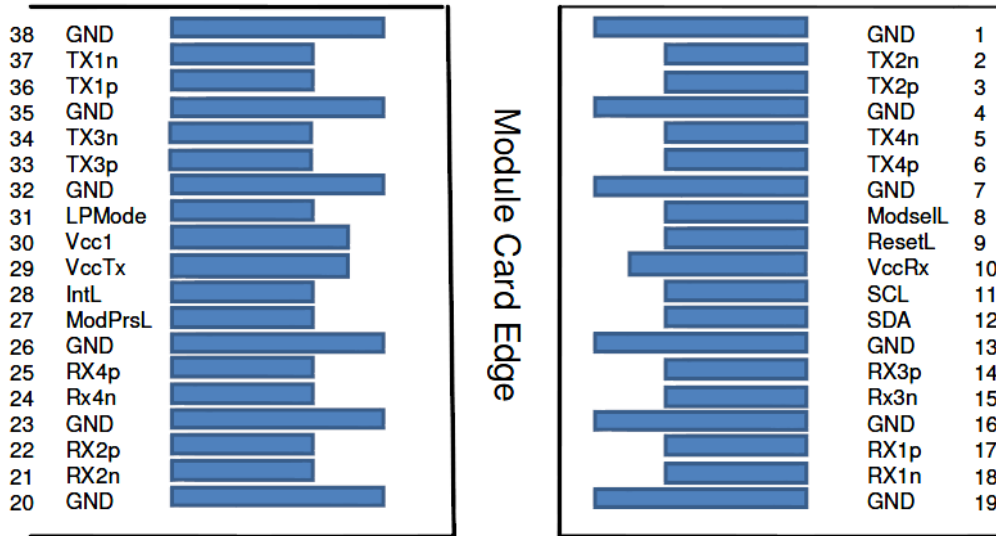
Receiver Optical Specifications					
Parameter	Symbol	Min.	Typ.	Max.	Unit
Lane Wavelength	L0	1294.53	1295.56	1296.59	nm
	L1	1299.02	1300.05	1301.09	nm
	L2	1303.54	1304.58	1305.63	nm
	L3	1308.09	1309.14	1310.19	nm
Signaling Rate per Lane	-	25.78125 ±100 ppm			Gbps
Average Receiver Sensitivity per Lane	Rxsens			-8.6	dBm
Average Received Power per Lane	RXPx	-11		3.4	dBm
Damage Threshold Per Lane	Pmax			3.4	dBm
Return Loss	RL			-26	
Vertical eye closure penalty, per lane				1.9	dB
Receiver electrical 3dB upper cutoff frequency, per lane				31	GHz
LOS De-Assert	LOSD			-13	dBm
LOS Assert	LOSA	-30			dBm
LOS Hysteresis		0.5	1.5	5	dB

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Electrical Specifications					
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.14	3.3	3.46	V
Module Power				4500	mW
Transmitter					
Input Differential Impedance	RIN	80	100	120	Ω
Differential Data Input	VIN	150		1200	mVp-p
J2 Jitter Tolerance	Jt2	0.17			UI
J9 Jitter Tolerance	Jt9	0.29			UI
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI
Eye Mask Coordinates {X1, X2, Y1, Y2}		0.11,0.31,95,350			UI/mV
Receiver					
Differential Data Output	VOD	300		800	mVp-p
AC common mode output voltage (RMS)				7.5	mV
Termination mismatch at 1MHx				5	%
Differential output return loss		Per IEEE P802.3ba, Section 83E-2			dB
Common mode output return loss		Per IEEE P802.3ba, Section 83E-3			dB
Output transition time,20% to80%		28			ps
J2 Jitter output	Jo2			0.42	UI
J9 Jitter output	Jo9			0.65	UI
Eye Mask Coordinates {X1, X2, Y1, Y2}		0.29,0.5,150,425			UI/mV

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7. Applications Note:



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin Definitions

Pin Assignment

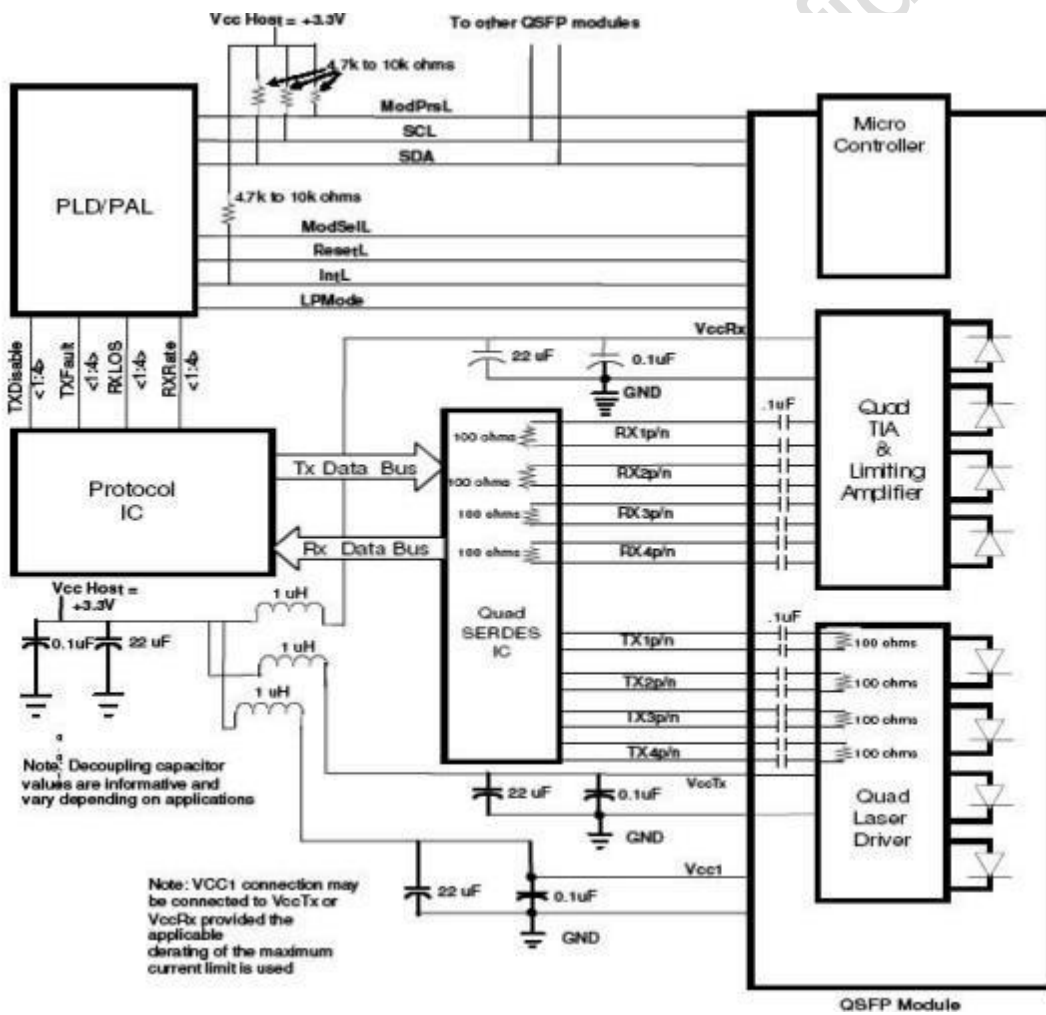
Pin	Symbol	Logic	Name/Description
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	3
3	Tx2p	Transmitter Non-Inverted Data Input	3
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	3
6	Tx4p	Transmitter Non-Inverted Data Input	3
7	GND	Ground	1
8	ModSelL	Module Select	3
9	GND	Ground	1
10	Tx2n	Transmitter Inverted Data Input	3
11	Tx2p	Transmitter Non-Inverted Data Input	3
12	GND	Ground	1

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13	Tx4n	Transmitter Inverted Data Input	3
14	Tx4p	Transmitter Non-Inverted Data Input	3
15	GND	Ground	1
16	ModSelL	Module Select	3
17	GND	Ground	1
18	Tx2n	Transmitter Inverted Data Input	3
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	3
22	Rx2p	Receiver Non-Inverted Data Output	3
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	3
25	Rx4p	Receiver Non-Inverted Data Output	3
26	GND	Ground	1
27	ModPrsL	Module Present	3
28	IntL	Interrupt	3
29	Vcc Tx	+3.3 V Power supply transmitter	2
30	Vcc1	+3.3 V Power Supply	2
31	LPMode	Low Power Mode	3
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	3
34	Tx3n	Transmitter Inverted Data Input	3
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	3
37	Tx1n	Transmitter Inverted Data Input	3
38	GND	Ground	1

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Recommended Application Interface Block Diagram



7. Modification History

Rev.	Comments	Date	Originator	Approval
01	Initial	2022.08.09	Albert Lin	Mike Sun